GREG MATURI
TENTMAKER SYSTEMS CONSULTING GROUP
consulting@tentmakersystems.com

Consulting
RTL and Architecture and Software for System, Board, High Speed and High Density FPGAs, ASIC design and verification. Experience with PCIe, FPGA, Xilinx, ISE VOIP, GPON,Video and Audio encoding and decoding., transport stream, Network protocols and SANs,IR imaging.

Proficiencies
VxWorks, RTOS, MIPS, Logic and Bus analyzers**,** MPEG**,** Verilog, Modelsim, MATLAB,Virtex-5,system Verilog VCS, ISE, Sypllify-Pro, TCL,Tk, PCI express, Quartus , ,Synopsys, Vera, C, C++,Java, SystemC, DSP, Image Processing, H.264, ATSC, DVB,GPON,ST7100, VOIP, . H.264, GPON, DSP, SoC, Perl,, Xlinx and Altera Design tools, Windows, Linux. Familiar with SMPTE Video and Audio standards, member MPEG committee, SCSI, and ATA, MATLAB, DSP, Quartus, Vivado, ISE , HDR, LED drive, algorithm development.

Experience

2010 -2018: Dolby Labs Senior digital designer.
2010: Consulting FLIR Systems
2009: Thinto Inc.- Founder
2009: Consulting Totalphase Corp.
2009: Consulting Dolby Corporation Santa Clara
July - December 2008: Consulting Intel Corporation Santa Clara
September 2007 – Jun 2008: Consulting Terawave Networks
September 2005 – March 2007: Due Diligence for Woodside Capital and Charter Ventures
September 2005 – January 2007: Consulting – NetLogic
October 2000 – Sept 2005: Propulsion Networks - Founder and Director of C/C++ Modeling of hardware
July 1998 – October 2000: Netergy - Design Manager
January 1997 – July 1998: Icompression Founder and CTO
May 1996 – January 1997: Luxsonor - Hardware Engineering Manager
June 1994 – May 1996: FutureTel/Innovacom: CTO/Design manager Compression products
January 1991 – May 1994: LSI Logic, DSP group, Head of DSP Audio group
March 1985 – December 1990: Lead Engineer, Texas Instruments, Advanced Guided Weapons
December 1981 – February 1985: Senior Design Engineer, Harris Corporation, Digital Moving Map Group

Education B.S.E.E. University of Virginia, December, 1981

Affiliations and Publications
Member of IEEE, ISO/MPEG Audio Ad-hoc group on Software Simulation,
ICCE Paper selection Committee,
Complexity Study group of MPEG 2 Audio ICCE , evaluated AC3 for MPEG2 .
Paper “250 MHz VOIP processor” presented at ISCCS 2000
Paper Decompression in German technical magazine Elrad.
Paper *Single Chip MPEG Audio Decoder* in 1992 International Conference on Consumer Electronics.
Limited Partner Charter Ventures

Patents
30 patents in DSP ,Image processing, Audio, IP , Memory,Networking ,VOIP and graphics.

Experience

DOLBY Labs *June 2010 to 2018:* Designed highly pipe-line architectures for Filters, pixel transformations, compression algorithms which were running at 300Mhz on AXI/APB buses with clock

gating for power optimization where required. Designed architecture, sub blocks and documentation on several generations of video processing FPGA and ASICS. Performed simulation, synthesis and debugging of video processing ASICS.
Wrote real time C code for HDR video processing display design on Linux. Developed and optimized algorithms for speed up. Designed ASIC and software for Fujitsu HDR camera, FPGA for HDR picture frame and advanced Professional monitor. Designed FPGA hardware and software for Pulsar professional monitor used for final mixing at many studios (used in Star Wars and Imaginationland), Designed FPGA and software for production HDR consumer monitor. Included TCON interface, Video processing, display interfaces, and developed and tested algorithms for LED local dimming to reduce power and video artifacts.

FIIR *January 2010 –June2010:* Designed and verified image processing units for Night Vision Sites. Verfied telemetry interface for interface to BMW . Developed and verified ethernet interface unit. Verifed and debugged flash interface bugs.

Thinto *2009 to 2010:* Brought up HDMI Board and Altera FPGA for repair and enhancement for Plasma Displays, using DSP and Image processing., H.246,MPEG2,and transport. Captured video and wrote C++ filtering programs.. Designed High speed I/O to standard high speed memory and Video chip. Wrote operational software and drivers for chip and debugged.. Used OpenGL and directFB displaying and editing streaming video.

Totaphase *April to July 2009:* Brought up Xilinx rocketio boards, USB 3.0 Analyzer, and FPGA development, ran bit error rate tests , coded in Verilog and VHDL for a high speed Video chip. Wrote software drivers.

Dolby 2009: Worked on Multi-Media Chip for enhanced plasma displays using DDR2 . Debugged DDR2 Interface for chip .Worked with AC3.

Intel 2008: July - December Consultant Worked on Multi-Media Streaming Video Chip MJPEG H.264 & PCI Express Interface . Debugged PCI Express interface , analyzed , integrated and synthesized MJPEG and H.264 modules and high speed interfaces.

Terawave September 2007 – Jun 2008: Consultant :Worked on Architecture and FDB for GPON system. Designed in Verilog for Altera FPGA's and ASIC ,.synthesized and debugged. Worked on forwarding hardware, hash table and error detection/correction.

Optvista August 2007- March 2007 Consultant Worked on Architecture, specs and coding for transferring VOD through FC, DVB, SDI, HD-SDI ,GE, OC48, DV6000 and Prisma, Some Verilog coding, estimated gate counts , writing Chip and FPGA specifications.

Woodside Capital and Charter Ventures
September 2005 – March 2007: Reviewed proposal for Woodside and gave a presentation to partners on Video application . Performed Due Diligence on Video over cell phone proposal and wrote up a presentation**:**

NetLogic
September 2005 – January 2007**:** Worked on Architecture, design, coding and testing of the 10 Mbit/s layer 7 processor, using Altera FPGA. Design included DDR2 SDRAM interface, TCAM Interface, and micro sequencers.

Propulsion Networks
October 2000 – Sept 2005: Founder and Director of C/C++ Modeling Developed Key architectures for Metro 10/40 Gbit chip (OC192/OC768). These included classification, high speed efficient memory architectures, Queuing, Input Buffering and Pre-classification. Headed up cycle accurate C-model development. Used C++ with sockets and a Java front end. Coded several C modules. Coded Verilog for several blocks of chip, including Queuing, caching and input stages. Verified these blocks. Helped develop SANs chip Architecture.

Netergy
July 1998 – October 2000: Architected advanced audio video processor (VP7) for Voice over IP applications. The SIMD /DSP architecture running at near 200MHz could outperform any of the top of the line DSP's for VOIP functions with much fewer gates. Coded 80% of the design, wrote C simulations and helped develop the emulator for software development. Designed memory subsystem block for T2 chip.

Icompression
January 1997 – July 1998: Co-founded company, wrote specifications and developed architecture for single chip MPEG2 audio/video/system decoder . Designed and tested more than 50% of the more than a million gate chip, from rtl to gate level. Developed c-code simulations to test chip. Wrote block level specifications for other blocks on the design.

Luxsonor
June 1996 – January 1997: Headed design team. Architect ed and coded several modules for an MPEG1, H.261, H.263 Codec, and developed c model for chip. Designed and coded several modules for a DVD decoder, including decryption block, Video filter scaler and PCI interface, and a sequencer with cache controller. Used modeltech VHDL and synopsis.

Futuretel/Innovacom
June 1994 – May 1996: Led design of MPEG2 Single chip Encoder: Developed Architecture, model and specification. Coded and tested several blocks using Verilog, C and synopsys. Performed Bandwidth calculations and algorithms. Wrote microcode.

LSI Logic:
November 1993 – May 1994: Designed VLD and Audio Core for combined MPEG2 video/audio chip.
January 1992 – November 1993: Led design team for MPEG audio core, AC3, and ATRAC and helping design an MPEG2 audio-video decoder chip.
July 1991 – January 1992: Designed single chip MPEG Audio decoder, including architecture, modeling, design and simulation. Modeling done in C. Design done in VHDL and MDE tools. Designed two spin-off products. Developed reduced size IDCT module for MPEG Video decoder.
January 1991 – June 1991: Designed MPEG Variable Length Encoder Decoder Module.

Texas Instruments
1989 – 1990: Headed Tracker Design team for guided missile program. Also responsible for VAX/Silicon Graphics/Hardware simulator which puts the Tracker hardware through a real time launch. I designed the architecture and several cards. Design included 1750 VHSIC processors, bit-slice array processors, SCSI, GPIB, RS232, and Silicon Graphics VME interface. I also wrote C, assembly, and microcode (for bit-slice).
1988 – 1989: Designed CPU and image processing card for hand-held battery operated launcher. Design included spatial and temporal filtering, scan conversion, and symbology insertion of 2 overlaid infrared imagers video. This card also controlled all control functions and external communications of the launcher. Design included RISC and embedded controllers, and Forth and assembly programming.
1987 – 1988: Designed lightweight, battery operated missile launcher. Design included DSP and image processing for the launcher display. Also designed ground equipment simulator and remote launcher. Some of the 14 unique cards I designed for this project included 2 processor card and their operational software.
1986 – 1987: Designed architecture and several boards for guided bomb. Video processing for the artificial intelligence required several CPU and Array processor cards, video, and telemetry cards. I designed the processor, video and telemetry cards and made changes to the array processor card to increase its throughput 7 times.
1986 – 1987: Led 5 man electronics design team for high-speed captive flight phase of advanced guided bomb. The unit consisted of about 20 cards, included CPU, DSP and Memory cards. I designed several of these cards.

Harris Corporation
1981 – 1985: Responsible for 4 of 12 of the cards for an F15 digital moving map. The 4 cards I designed implemented a JPEG-like video compression algorithm.