PAUL B. BROWN
TENTMAKER SYSTEMS CONSULTING

OBJECTIVE:

A challenging consulting position developing digital hardware and/or leading a team in the development of digital hardware.

TECHNOLOGY/TOOLS SUMMARY:

HARDWARE: CMOS gate and standard cell arrays, Xilinx 3000, 4000, and Virtex series FPGAs, Vitesse GaAs Crosspoint Switches, TTL and ECL discrete logic.
LANGUAGES: Verilog, VHDL, C, Perl, Tcl.
EDITORS/UTILITIES: vi, emacs, nroff, Framemaker, Microsoft Word, Clearcase, sccs, vcs, make.
CAD: Verilog (Verilog-XL, VCS), Virsim, Signalscan, Synplify Pro, Leonardo Spectrum, Synopsys Design Compiler, PrimeTime, SureCov, Mentor Graphics Design Architect, ORCAD, Xilinx tools, Samsung ASIC tools (design rules checking, timing analysis, test vector extraction, etc.).

PROFESSIONAL EXPERIENCE:

Philips Semiconductors, San Jose, CA 1/2003-3/2003
Independent Consulting Engineer

- Mapped the Verilog coded design of a multi-million gate 802.11 SoC IC to a set of Xilinx FPGAs. Re-partitioned the design to fit into two large Virtex2 FPGAs. Modified the design as required to use Xilinx specific elements (embedded RAMs, multipliers, and I/O cells). Used Xilinx Coregen to create the BRAM and multiplier cores.
- Synthesized the design using Synplify Pro. Identified, and communicated back to the IC design team, logic and timing problems in the "source" IC design.
- Used Xilinx Map and PAR tools to implement the design. Simulated the resulting gate level implementation.

Intrinsix Corp, Milpitas, CA 1998 – 8/2002
Principal Design Engineer

Intrinsix is an engineering services company. During this time worked on projects for a number of clients.

- Microsoft (WebTV) (2+ years) –. Developed a number of functional units used in a DSS/JPEG Transport Stream processing ASIC, including a DMA engine and a PCI Bus interface. This chip was implemented using a Samsung .25 micron, 500K gate (plus RAM) standard cell part. It had multiple clock domains running at up to 80 MHz. Did design and unit level simulation using Verilog. Used Chrysalis formal verification tools to check for proper asynchronous clock boundary crossings, and SureCov for simulation coverage analysis. Was responsible for top level integration of all units including I/O cells, for gate level simulation, and for chip level backend processes including synthesis, timing analysis, design rule checking, and test vector extraction. Helped bring up prototypes. Also worked on parts of several other ASICs.
- Hewlett Packard (PICO Project) – Worked on an interface between a hardware accelerator core and the outside world. Successfully developed an AMBA AHB to PICO Bus bridge in a short time. Wrote a specification, and coded the design in Verilog. Also developed an AMBA AHB simulation environment.
- Lucent (ORCA Design Center) – Provided customer support for ORCA FPGA customers. Analyzed several ORCA customer designs looking for speed improvements. Developed a high-speed FIFO hard macro. Took an existing PCI interface design and created a hard macro to be used by a customer.

- COE Manufacturing Company – Assisted with the development of the Image Pre-Processing board. This board included an embedded processor several interfaces and two Xilinx Virtex FPGAs. Designed

and captured a portion of the board using ORCAD. Took the FPGAs through synthesis and place and route. Assisted with verification and board bring-up.
- Steptech – Developed the Verilog code for two Altera FPGAs working from customer specifications. These formed the core of the control section of an ATE system analog instrument.

Credence Systems Corporation, Fremont, CA 1996 - 1998
Senior Staff Design Engineer

- Developed the scan vector generator module for an ATE system which provided vectors for up to 32 scan chains at 100 MHz. Generated a specification and modeled the design using Verilog.
- Implemented the design using DRAM arrays, a CMOS ASIC, GaAs crosspoint switches, a Xilinx FPGA, and discrete ECL and TTL logic. Mentor Graphics tools were used for schematic capture and layout. Performed board level timing verification and adjusted trace lengths of all signals to meet speed requirements (10 nsec cycle time).
- Supervised layout of the 20 layer PCB, addressing such issues as component placement, PCB stackup, trace widths, etc. Specified board level diagnostic testing. Successfully brought up the first prototypes.

ASCOM, Nexion, Acton, MA 1994 - 1996
Senior Engineer

- Developed various elements of an ATM switch, including link flow control, multipoint to point arbitration, cell processing and formation, and various aspects of record handling and buffering.
- Incorporated these functions into two large CMOS ASICs, the Bandwidth Arbiter chip and the From Switch Port Processor chip. In each case was responsible for about half of a VLSI Technology 180K gate device.
- Implemented these functions using Verilog. Built test benches for verification at the function level, and used a system level test bench to do further verification. Assisted the design verification group and evaluated the results of a coverage tool.
- Helped modify Verilog code and the floor plan to meet timing requirements.
- These ASICs were successfully incorporated into a product that was brought to market.

Kendall Square Research, Inc., Waltham, MA 1993 - 1994
Senior Engineer

- Responsible for the development of the Cell Interconnect for a massively parallel super computer. This function provided the interface between each computing cell and the ring bus structure which interconnected these cells. The central element of this function was a shadow cache.
- Made area versus performance tradeoffs, developed a specification, and generated a Verilog model prior to the project being canceled.

Sequoia Systems, Inc., Marlborough, MA 1987 - 1993
Senior Engineer, Group Leader

- Worked with the system architect to develop the structure of key elements of the I/O subsystem for a fault tolerant computer. Wrote a detailed specification for these functions.
- Developed a complex DMA engine which acted as an interface between main memory and the I/O subsystem. Used Verilog and Synopsys Design Compiler to implement the design in a LSI Logic 25K gate CMOS ASIC.
- Worked on a VMEbus interface and wrote a Verilog model for a complex VMEbus controller chip.
- Responsible for the I/O subsystem Verification.

EDUCATION:

B.S, Electrical Engineering, San Diego State University.

B.A., Fine Arts, San Diego State University.
Graduate level courses in computer science, Harvard University, Division of Continuing Education.
Verilog Advanced Techniques and Behavioral Modeling (Cadence).
Synopsys Logic Synthesis 2 Workshop (Synopsys).

MISCELLANEOUS:

Contributor to the Book, *Timing Verification of Application-Specific Integrated Circuits* by Farzad Nekoogar, specifically, Chapter 4, "Programmable Logic Based Design".

U.S. Patent Application: Transport processor for processing multiple transport streams.
U.S. Patent Application: Dynamically variable track size in a DASD cache.