NEIL MAMMEN
TENTMAKER SYSTEMS CONSULTING GROUP

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Hands On System/Chip Architect and Technologist, Chip & New Product Specification and Architecture, Board/System/Product/FPGA Architecture & Design. Technical Marketing and Evangelism assistance. Product Applications Boards, Reference Designs and Support. ASIC Verification and Validation boards and FPGAs.

Some Accomplishments and Skills:

Experienced CTO & Vice President of Engineering and R&D

Experienced Video Systems Architect

Skilled (with practical experience) in taking concepts, algorithms and customer requirements and creating a manufacturable System or ASIC architecture; and then driving it through design to completion. Also skilled at presenting and gaining customer (and VC) confidence and loyalty through training, presentations and interaction.

Experienced High Density and high speed FPGA Architecture and Verilog Design. Altera and Xilinx.

Experienced Systems and Board Architecture, Design, Bringup Debug etc.

Experienced Chip/ASIC Architect.

Experience with ASIC Functional Verification targeting very large FPGAs.

Successfully delivered PCIexpress and High Speed Serdes FPGA and board design projects.

Co-founded and raised $14.5M VC funding for an ASIC startup company in 2001 after the markets had crashed.

Conceived and architected the world's first ***Clear Channel*** 40G Layers 2-4 Network Processor ASIC multichip set. Design scales down to provide a Clear Channel 10G Network Processor. Took design through funding, recruiting, Micro-Architecture and a functioning cycle accurate C-Model. Authored and applied for 16 patents in multiple areas including Memory Bandwidth, Statistics Collection, Network Processing, Traffic Shaping etc.

Architected a 32G SAN switch chipset for company's new direction. Two new patents started but not filed due to company closure.

Co-designed, Product Planned and Specified the world's first ever MP3 player chip in 1992.

Architected a large 200+ card Optical DSL system as a consultant. Design was built and deployed. Co-author of the patent submitted based on my Architecture.

Called in for Emergency Consulting. Prior 4-man team had taken 6 months and hadn't been able to get high speed MAC design to work. Threw away entire prior architecture and started design from scratch. Single handedly re-architected, designed, implemented and debugged and reliability tested in 6 weeks, a complete 1G Backplane Proprietary IP Packet MAC in a space and speed limited FPGA at 125MHz for a Metropolitan Area Network (MAN) implementation. This allowed company to show working systems to customers on schedule. This FPGA had about 8 flavors created and used in every one of companies

Networking blades. Expanded above design to provide a 2.5G MAC in an FPGA with internal speeds of 156MHz DDR. This allowed company to ship their 2.5G MAN products ahead of anyone else.

Co-author of two Luminous Networks patents in Metro field relating to Traffic Shaping and Reliability.

Designed and implemented FPGAs incorporating, I2S audio, VESA VIP and SPDIF standards.

Architected an OC192, Video Aware IP Network Processor. (Preliminary Specifications and Block level). The startup company raised money partly on this architecture.

Responsible for Engineering Department of 40 engineers and technicians and documentation, taken over from old VP of Engineering who was discharged.

Proposed, architected, designed, submitted RFP and delivered the *winning* SouthWestern Bell MPEG2 Deployment System solution. System was manufactured and deployed for testing.

Proposed, architected, designed and submitted RFP for the *winning* Hong Kong Jockey Club MPEG2 Deployment System solution, competed and won out against IBM (we were using their own chipset against them).

Proposed, architected and designed and delivered the *winning* NORTEL DV-45 MPEG2 Codec contract.

Proposed and architected a MPEG2/ATM Multi-Re-multiplexer System solution for major European Telco.

Came up with the concept and wrote initial product requirements & specs of the iCompression MPEG2 codec chip. The worlds first single chip Audio/Video Data Encoder and TS Mux chip. Conceived of and identified the strategic need for a single chip multi-featured codec and was instrumental in locating the founders and helped promote and finance the company through NUKO Information Systems. ICompression was later sold for $500M to Globespan. The resulting product is a current Single Chip encoder and it's derivatives that are being sold today.

Within 4 months of joining start up (unpaid), hired and motivated 3 engineers (also unpaid), architected, designed, laid out, manufactured and debugged 2 new boards and 2 reference designs, to prototype a 7 channel real time MPEG 2 encoder and decoder to demonstrate the *world's very first* multi-channel MPEG 2 codec to work over DS3 for a Pacific Bell NAB demo. This was the worlds first video transmission of MPEG over DS3 and the first application of distance learning (Stanford University to Las Vegas NAB).

Architect and primary FPGA, Board and System designer of the NUKO Highlander MPEG 2 System. Includes the MPEG 2 Multifunction Transport Stream Multiplexer and the NUKO Highlander MPEG 2 Multifunction Decoder. System includes multiple redundancy utilizing on board Alarms, redundancy SW, SNMP, GUIs etc.

Creator of the "Mammen" VME Hotswap Methodology, before there was a VME64 Hotswap. Used successfully and reliably in the NUKO Highlander System with 0 failures in 4 years. Units in use are still running years later

Architect and primary designer of the NUKO IBM MPEG 2 Encoder solution.

Co-Architect of the Multistream ATM Trunking Multiplexer and DeMultiplexer. Allowed the use of up to 9/36 MPEG 2 multi-rate bandwidth streams to work on OC-3 lines over ATM framing, with multiple redundancy.

Sole applications engineer for the *world's first* C-Cube MPEG 1, "1+" & 2 Encoder chipset and microcode. Supported over 25 customers (simultaneously) in enabling them all to come to market with Real Time

MPEG 1, “1+” and 2 Encoders. At one point in time, of the 17 production MPEG encoders available in the world, had helped design and debug 15 of them.

Helped specify new product features and requirement for an MPEG Audio encoder vendor (that I was unaffiliated with but needed for a product of my own). This audio encoder module proved to be an enormous success for that company.

As a newly hired applications engineer at C-Cube, within 2 weeks, discovered and designed work around for an interface flaw in primary product that 2 previous applications engineers and the chip's own design engineer had spent 4 months trying to find. Fixing this problem resurrected a key design with a key customer and allowed us to correct our Technical Manuals. Problem detection included having to evaluate original VLSI design and state machines.

Through my direct intervention, effort and management resurrected and maintained a critical NRE account worth over $500,000 just when the company thought we were going to lose it all.

Came up with an innovative work-around to help crucial customer get to market ahead of schedule before critical inverse telecine microcode was available.

Debugged new chip revision to discover critical temperature issue, which further explained other failures to date. This was a bug that had plagued the company before I attacked the problem.

Product Planning for *world’s first* LSI Logic Audio MPEG 1 Decoder Single Chip. Defined features set, designed Evaluation board and wrote software. Provided Technical Seminars for Customers and FAEs. Chip forecasted over $10 Million in sales within the first 2 years. Wrote Technical Manual.

Applications support for LSI’s first generation CCITT H.261 video chipset. Joined division and within a month, implemented a last minute mask fix on the existing chipset to make it reliable. Included recommending a new spin of the old chipset to correct system I/F problems and bugs.

In 4 months started up and established a fully functional applications group to support new SPARC RISC chipset, SparKIT. Hired and trained 9 engineers. Developed evaluation boards for customer training and chip debug, installed Customer Hotline, databases, started FAE magazine, FAEdback, etc. COMDEX shows, developed and produced customer training seminars around the world.

As manager of the SPARC Applications Department was responsible for design and manufacture of boards, chip specifications, product planning and debug of chips for the SparKIT-25 and 40, IU, FPU, MMU and Peripherals to the Mbus and SBus. Included the assist of debug and porting of SUN OS 4.1 to the new MMU and peripherals. Other support products included SUN OS and the original chips in the SUN SPARCstation 1, 1+, 2, IPC etc. and their clones. Responsibilities included SPARC International compliance test suits. Responsible for training FAEs and sales force on our chipsets as well as competitor’s chips.

Established, stocked and managed fully functional lab for 3 divisions, (SPARC, MIPS & DSP), included set up for customer demos as well as setups for customer board debugging and support.

Responsible for production and content (with Tech Pubs) of entire line of SPARC Technical Manuals and Data Sheets for above products. We produced over 20 publications of which 11 were Technical Manuals.

Worked with 12 PC manufacturers to enable them to create the first SUN SST1 (SPARCstation 1) and SST1+ clones.

Taught RISC Microprocessor/System technical seminars around the world in cooperation with SUN Microsystems.

Set up documentation procedure to allow the sign-off, control, production and update of technical manuals, errata and appnotes through-out the world. Included the "FASTfax" system to immediately getting critical applications and errata information to customers without having the delay of going to Tech Pubs. System was later standardized and adopted by other divisions.

With engineering partner, discovered only way to correct more than $100,000 worth of already manufactured TAXIchip™ parts. Saving inventory, customer loyalty, future sales, and company's public image.

Primary, world-wide Application Engineer for the AMD TAXIchip™, 125 MHz high speed, point to point I/F chipset. Wrote the TAXIchip™ Technical Manual, designed the MINIcab™ and TAXIcab™ boards. Wrote specs, assisted customers in their designs and designed future products. Taught TAXIchip™ seminars around the US. The TAXIchip is currently an industry standard of sorts.

In 45 days designed an NTSC high speed 2 Km fiber optic video digitizing board for key customers, a major show, seminars and engineering publications, resulting in major sales and publicity. This system is now being used in a slightly modified form by various customers for security cameras as well as by airline companies for personal video entertainment at your seat.

Authored and gave TAXIchip™ seminars given throughout the US.

Coordinated and organized transfer of manufacturing between wafer fabrication areas. Saved company over $1,000,000 in fab operational costs.

Other Skills and Tools: Xilinx, Altera, Pascal, C, FORTRAN, PL/M, Assembly Languages, PALASM, CUPL, ABEL, various Schematic Entry and FPGA development packages, AHDL, Verilog, StateCAD, Synplicity, ModelSim, VCS, Silos III, OrCAD, PCAD, BASIC, PIC BASIC.

Other Activities: Motivational Speaking, Training individuals to give effective presentations, Training lay people to be effective speakers and preachers, Video Editing and Production, Audio Production (I Witness Band: Piercing the Darkness, 1991; Victory, 1993; At the Cross, 1994), Teaching and Preaching Apologetics and Theology.

"MOD Night" Once a year, coordinate and manage an extracurricular activity involving over 120 volunteers and over 380 Junior High kids in a one/two night "Outward Bound" style Night Game activity spread out around the Santa Cruz , CA or Portland, OR mountains.

Quick Architecture and Design Summary (Boards and Systems and FPGAs, unless indicated includes design as well as architecture as well as FW, SW and Systems architecture and support. Unless noted, systems were shipped for revenue), covers items mentioned above as well:

TAXIcab : TAXIchip Circuit Application Board
TAXIvideo : TAXIchip Video Transmission Board
Saavik 1 & 2 : LSI Logic MPEG 2 over DS2 ISA Decoder board.
Spock I : 9U VME Audio/Video Multiplexing board
Spock III : 8 input Transport Stream Multiplexing board designed using FPGAs.
Sarek III : 9U VME C-Cube MPEG 2 Encoder board. Multiple FPGAs.
DV-MPEG : Hot-swappable NORTEL Chassis Codec System (6U) consisting of the 4 boards below.
- Riker : IBM MPEG 2 Encoder board
- William : Hot-swap NORTEL Motherboard for above Encoder.
- Troi : C-Cube Decoder Board
- Deanna : Hot-swap NORTEL Motherboard for above Decoder.

Atlas : 9U VME Fully Redundant mother board for a full featured Codec
Atlas III : 6U VME Fully Redundant mother board for a ultra full featured Codec (not manufactured)
Sammy : 9U VME Video Input, Audio Encoder, MPEG TS muxer board

Uhura : 9U VME 9 channel ATM TS multiplexer over OC3c or DS3
(Specifications and co-architect)
Aruhu : 9U VME 9/36 channel ATM TS demultiplexer over OC3c or DS3
(Specifications and co-architect)
Sulu : 9U VME Full Featured Video Input, Audio Encoder, MPEG TS muxer board
(not manufactured)
XIM : Low cost ATM Transmit and Receive module for above systems (not manufactured)
DV3000 : 6U MPEG Codec System (not manufactured)
Highlander : Multi-Redundant 44/40 U chassis 9 channel 9U Codec system
Spock VIII : Single chip 8 input/8 data Transport Stream Multiplexing ASIC/FGPA solution
(not manufactured).
ICompression Single Chip Encoder
: Primary Systems level definition for the ICompression Single Chip MPEG 2 Encoder, also initiated the founding of ICompression to provide me with a substitute for the C-Cube encoder.
Picard : ICompression Encoder PCI board.
ReMuxer : Architect of the MPEG2/ATM Multi-Re-multiplexer System and Chassis
(not implemented).
TPM1 FPGA: DIVA Systems Transport Processor Module,
Completely re-architected and redesigned their Transport Processor FPGA.
TPMII : DIVA Systems Transport Processor Board II.
Architected the second generation of the DIVA board for Video On Demand. Architected and designed the core FPGA, the M4SPROC, a 4 stream MPEG TS processor.
TPMtester : DIVA Systems Tester board.
Architected, designed, debugged this large test board with multiple connectors and connections to allow a fast test and bring-up environment for the DIVA TPMII boards.
DVB2MII : Luminous Video TS DVB to Ethernet Board including all FPGAs. Implemented a module to convert and reconvert Video TS to IP over Ethernet to allow it to be transmitted over any 100baseT network. Board and FPGA being used for demo systems at shows and was used to capture a critical investment.
LMAC 1G : Luminous Backplane MAC FPGA. Multiple flavors of this FGPA are being shipped in all Luminous Products, with multiple per card and upto 6 on the Switch Card.
LMAC 2.5G: Luminous Backplane MAC FPGA. This FPGA is being shipped in all 2.5G Luminous products.
VIP Interface: FPGA that interfaces MPEG TS and I2S and SPDIF to a VESAVIP bus.
PCI to HPI bus interface: FPGA that interfaces PCI to local bus. Includes CCIR656 Interface to PCI, interface ensures ability to preview with VCR FF and REW inputs.
PCIexpress Northstar III: Implementation of Xilinx core for proof of concept. Done in 12 weeks to demo with working video.
PCIexpress FPGA/ASIC Verification suite of boards: Validation of PCIe and Video ASIC RTL in FPGA
PCIexpress ASIC board: Validation board for PCIe ASIC chip with video
Multiple other PCIe designs.

Background Summary:

Tentmaker Systems Consulting: 2002-Present

- Xilinx Inc.
- Philips/NXP Semiconductor (various groups within Philips)
- WIS Technologies (various fill in roles within WIS)
- Multiple other companies.

Propulsion Networks: 2001-2002

- Co-Founder, Chief Architect and VP of Technology.

Conceived, Proposed, Defined and Architected a Metro/Core Router 40G/10G Network Processor. Raised $14.5M. All schedules met. Fully functional gate level C-Model demonstrated. Received lots of customer enthusiasm and validation. Author of 16 patents (some still being applied for).
Despite meeting all our goals, due to delayed market for 40G Network Processors, the VC's opted to close down the company and sell off the IP to Altera.

Luminous Networks: 2000-2001

- Was consulting - joined at the request of the CTO and CEO
- Principal Architect, Office of the CTO
  Co-Author of 2 patents
- **Director, ASIC Design.**
  Took over the ASIC group till I was able to hire someone to replace me at the request of the CEO.
- Left to start my own company as per my prior agreement with the CTO.

Tentmaker Systems Consulting: 1998-2000

- Xalted IP Networks 2000
- Luminous Networks 2000
- Azanda Microsystems 2000
- DIVA Systems 1998-2000
- Cradle Technologies 2000
- Pulsent Technologies 1998-2000
- Dynachip 1998
- ShivaSAT 1998
- ADC Communications 1998

NUKO Information Systems: 1994-1998

- Chief Technology Officer & VP of Engineering 1997
- Chief Technology Officer 1996
- Chief Technologist 1995
- Director of Engineering 1994

Tentmaker Systems Consulting: 1994

- NUKO Information Systems 1994

C-Cube Microsystems: 1992-1994

- Manager, System Design and Applications
- Senior Staff Applications Engineer, System Design

LSI Logic: 1989-1992

- Senior Staff Member, Applications, DSP Division.
- Manager, SPARC Applications Engineering

Advanced Micro Devices: 1984-1989

- Senior Product Planning and Applications/Strategic Development Engr, High Speed Serial Interface/Optical/Networking Development Group.
- Product Engineer, Microprocessors Division.

Spectra-Physics: 1982-1984

- R&D Associate Engineer, Laser System Division (Eugene, Oregon) Electronic Design and Interface.

UC Berkeley Extension: 1987-1994

- Taught Digital Logic Design and Digital Logic Design Lab. Highly ranked by Students Surveys.

Education:

- MSEE 1984 Computers and Solid State Physics, Oregon State University.
Masters Degree Thesis: A Bit Slice Microprocessor Learning System
- BSEE 1982 Electrical and Computer Engineering, Oregon State University.

Societies and Awards

- President, Tau Beta Pi OR Alpha Chapter 1983
- Eta Kappa Nu
- Chairman of IEEE Student Organization 1984, OSU
- Teaching Assistant of the Year Award 1984, OSU (Electrical Engineering Department Students)
- Wyle/EE Times American By Design Contest, 1st Place Design Winner for Digital Devices. 1995.
- Wyle/EE Times Idea Quest Grand Prize Winner 1997. Winner of the Saturn EV1 Electric Vehicle.
- NUKO Summit Award 1995 Most Valuable Employee Voted by all employees.
- NUKO Summit Award 1996 Most Valuable Employee Voted by all employees.

Other Skills: Special Event Motivational Speaker for Corporations
Apologetics Speaker at various Churches and Conferences around the world.

Business and Personal References:

Jayshree Ullal,
VP Marketing, CISCO Systems

Bob Kondamoori,
Previous Position: CEO and Chairman of the board, NUKO Information Systems

Ram Kedlaya,
Previous Position: VP Business Development, NUKO Information Systems

Personal Reference: Pastor Bill Buchholz
Senior Pastor, Family Community Church

Additional References Available on Request