JOHN F. EATON
TENTMAKER SYSTEMS CONSULTING

Hardware design engineering Consultant (analog/digital) for electronic systems, circuit boards,ASICs, CPLDs, and/or FPGAs.

Summary of Qualifications

Extensive hardware design experience (analog/digital) with circuit boards and systems. Recent design experience with validation boards testing complex network ASICs, including: a Media-Access-Controller (MAC) for Gigabit Ethernet, a Network Controller for voice-over-IP with Asymmetrical-Digital-Subscriber-Line (ADSL) interface, and a Reconfigurable-Communications-Processor for cellular phones and antennae. Past hardware design experience with network PHY interfaces, high-speed buses PCI/VME/EISA), ADSL, MPEG-2, NTSC video, audio, 32-bit microprocessors, Digital Signal Processing (DSP), real-time image processing, real-time spatial filtration (2D FIR), Digital-Subtraction-Angiography (DSA), and Computerized-Axial-Tomography (CAT). Recent programming experience with ALTERA CPLDs using VHDL/Verilog.
Past programming experience with board-level testbenches (VHDL) and C programs that simulate image processing hardware. Educational background includes an MSEE (analog/computer science) with Distinction and Departmental Honors, an extensive collection of post-graduate courses in high-technology subjects, and a Certificate in VLSI Design Engineering with A's and one B.

Education

1995, Univ of Calif., Santa Cruz (VLSI Design Certificate)
Courses: Verilog, Synopsis, FPGA Programming, VLSI and ASIC design, VLSI Testing, Formal Hardware Verification, Principles of Image Compression.
Grades: A's with one B.

1974-1995 Post Graduate Courses (Electrical Engineering); Schools: UC; UCLA; USC; SJSC, Foothill College, Battelle Institute; Courses: DSP, Image Processing, Software, Computer Graphics and Engineering Management.

1973-1974 Calif. State Univ., San Jose; MSEE: (Analog Circuit Design/Computer Science)

1958-1962 Calif. State Univ., San Jose; BSEE (Electrical Engineering) with Distinction & Departmental Honors; Math Minor; Honor Societies: Tau Beta Pi(engineering), Tau Delta Phi (scholastic)

Professional Experience (Recent)

2001 - 2001
Chameleon Systems, Inc., San Jose, CA
Senior Hardware Systems Design Engineer

Chameleon Systems is a fabless chip company designing a reconfigurable-communications-processor ASIC targeted to cellular applications, such as phones and antennae. The processor is unique for its ability to be reconfigured at the beginning of a clock cycle based on instructions from application code. Reconfigurability allows OEMs to optimize processor resources for maximum speed and minimal cost.

I was part of the Hardware Systems Group. My initial responsibility was writing a Hardware Design Guide, allowing an OEM to fast-track their ASIC design to a board-level application.

My hardware design responsibility was designing a 10-layer circuit board for validating the operation of two reconfigurable-communications-processor ASICs in a master-slave configuration. The clock speed of the ASICs was 100 MHz. The board featured a PCI bus interface, an INTEL 21150 PCI bridge ASIC, 2

XILINX FPGAs (XCV400 VERTEX), two MAXIM (MAX1638) 20-amp switching regulators, MICRON SSRAM and SDRAM, and two PMC (daughtercard) interfaces.

1999 - 2001
ishoni Networks Corp. , Santa Clara, CA
Senior Hardware Design Engineer

ishoni Networks is a fabless chip company designing and marketing ASICs that function as Broadband Network engines, allowing OEMs to provide residential and business customers with secure voice and internet services over a single broadband connection. The company recently sold a majority interest (51%) to Philips Electronics, Inc.

The company's first ASIC had interfaces (network, bus, and memory) for PCI, TDM, UART, HDLC, I2C, USB, HOST (MOTEL), UTOPIA, SDRAM, PIO, MII, 10/100 Ethernet, EJTAG, and T1/E1. The second ASIC had most of the previous interfaces plus an ADSL (Asymmetric Digital Subscriber Line) interface.

I was part of the Hardware Systems Group and designed two bring-up boards for testing and validating the company's broadband ASICs.

For the first board, I wrote the specification, defined the architecture, designed the circuitry, layed-out the board, wrote most of the code for four CPLDs, wrote the test procedure, and was heavily involved with the test and validation of the broadband network ASIC itself. The project included interfacing and testing the signaling and protocol of the earlier mentioned interfaces.

For the second board, I wrote the specification, defined the architecture, designed the circuitry, and created the schematic (VIEWLOGIC) and parts list. My efforts included designing an analog front-end (AFE) daughter board for the ADSL interface. The design of the second board included a Bit Error Rate Testing (BERT) capability for validating the ASIC's long-term ADSL reliability.

1998 - 1999
Xaqti Corp. , Santa Clara, CA
Senior Hardware Design Engineer

Xaqti Corp. was a fabless chip company that designed and marketed Media-Access-Controllers (MACs) ASICs for Gigabit Ethernet. It has since been sold to Vitesse Semiconductor , Inc

I worked in the Hardware Systems Group and was responsible for testing and validating the company's ASICs.

I contributed to the design of two bring-up boards that tested and validated the company's ASICs.

My design duties included writing VHDL code for six ALTERA CPLDs. Two of the CPLDs served as the pass-thru interface of the AMCC 5933 PCI controller chips on each board. Four of the CPLDs served as read/write interfaces to the ASICs themselves and to the ASIC's data-packet memories. I was also heavily involved with the ASIC validation effort. To support this effort, I wrote a board-level testbench (VHDL) using a ModelSym hardware simulator. The testbench was invaluable for confirming and troubleshooting the logic and timing problems with the ASICs.

I worked briefly designing a Gigabit Ethernet switch (board) that functioned as a stream interface (switch fabric) for several Gigabit Ethernet MAC ASICs. The board functioned as a switch emulation platform for the chips pre-silicon, and as a hardware reference design and testing platform for the chips post-silicon. The design used several Octal 10/100 MACs and several Gigabit Ethernet MACs. I wrote the VHDL code for the stream interface controller and created a schematic in ORCAD.

1995 - 1998
NUKO Information Systems , San Jose, CA
Staff Engineer

NUKO Information Systems designed and manufactured broadcast-quality MPEG2 (audio/video) encoding systems. Their largest system contained multiple encoding channels and was housed in a ruggedized, 21-inch, 7-foot tall rack. NUKO's typical customers were operators of satellite head-end facilities.

I shared responsibility for the VME bus interface design (digital) of the video/audio multiplexer board in the encoding systems. My tasks included the design of the digital logic and writing VHDL code for several ALTERA CPLDs.

I improved the reliability of the synchronous control bus for the video encoder chips (C-Cube) on the video encoder board. My tasks included troubleshooting and re-programming several CPLDs.

I designed (analog/digital) the hot-swap interface for the VME bus. This effort included designing hot-swap interfaces for two redundant SPARC CPUs and designing the hot-swap interface for all the boards in the system. The major hot-swap components included power FETs for switching power to the boards, hot-swap bus transceivers (specifically designed for hot-swap), QuickSwitch bus isolators for switching VME bus signals, an embedded processor (8051) for controlling the switching of the redundant SPARC CPUs, a UART for communicating with the SPARC CPUs, multiple MAXIM voltage monitors for triggering hot-swap control sequencing, and multiple ALTERA CPLDs for interfacing the hot-swap circuitry.

I designed the analog preamplifiers for the video/audio encoder board. The design used op-amps and ASPI (Atlanta Signal Processor, Inc.) audio encoders.
I designed an enhanced analog preamplifier for the next-generation video/audio encoder board. The preamplifiers featured software programmable gain and attenuation. The preamplifier used op-amps, VCAs, DACs, TCRs, a Howland current source, and ASPI (Atlanta Signal Processor, Inc.) audio encoders.

I worked on improving the video quality of the system. I taught an NTSC video theory class.

I wrote an audio test procedure for the system that used a Tektronix AM700 Audio Measurement Set.

1995 - 1995
Univ. of Calif., Santa Cruz , San Jose, CA
Full-Time Student (Extension)

Degree: Certificate in VLSI Design Engineering Certificate Courses: Verilog, Synopsis, FPGA Programming, Fundamentals of VLSI and ASIC design, VLSI Testing, Formal Hardware Verification Non-Certificate Course: Principles of Image Processing Standards (MPEG-2) Grades: were As and one B.

Hobbies

Oil and watercolor painting, jogging