NEIL MAMMEN

Neil3 at tentmakersystems.com

ARCHITECT, INNOVATOR, HW ENGINEER & TEAM MOTIVATOR
BRINGING DIVERSE TEAMS AND TALENTS TOGETHER TO DELIVER RESULTS

Customer focused Technologist, System Architect,
PC Board, Chip, FPGA, Architect & Designer

Evangelist and VC fundraiser

- As CTO helped raise over $70M in VC and Investment Funding for NUKO Information Systems
- Co-founded and raised $15M VC funding for startup Propulsion Networks
- Co-founded and helped raise $3M VC funding for startup Bay Microsystems

End to end execution

- Conceived & created requirements based on Customer needs, Architected, Raised Funding, designed and executed multiple products. Understand how to isolate, nice to have features from must have features as well as staging minimally viable features for the greatest impact.

Vendor Relationships and management

- Long term experience & relationships with prototype manufacturing and assembly facilities for Lean Startup quick turn boards in US, & medium turn & small-scale production in China. Includes interfacing and managing all aspects of prototyping, layout, fab, procurement, assembly, bring up, debug, rework etc.

Innovator & Architect

- Over 18 Patents (granted or pending) in various fields (Intel, Dolby, Luminous, Broadcom etc.).
- 7 of the above patents are now Intel NPU/CPU Architecture patents (potentially more in the pipeline)

SOME ACCOMPLISHMENTS

Assembled from scratch and managed teams of over 40 Engineers, Technicians and 100 person staff as CTO and VP of Engineering to deliver complete end to end products, including creating and managing documentation and library systems.

Architected and led development teams for implementation for large projects contracted to us for customers such as Netlogic (Broadcom), Xilinx, Philips Semiconductor, JDSU, Brilliant, Jolata, Xalted, Varian & Mentor. Included all phases, from Architectural proposals, design, management of multiple engineers, board layout, fab, assembly, part procurement, testing etc.

Moved corporation from a single Software Application provider to a full Hardware/Software/Systems platform, by architecting a completely new Video Deployment System. Then used this architecture to capture multimillion-dollar systems level contracts from Pacific Bell and Nortel to deliver the very first Video Services over their networks.

Based on an idea I had, met with customers and network providers to architect the first 40G Network Processor, then raised 15M from Venture Capital and hired staff and engineers to develop chipset.

Worked with software centric technologists to architect a new Layer 710Gbps DPI chip for cybersecurity applications that was expected to exceed $70M annual run rate in full production for Netlogic/Broadcom. Recruited and guided Team to implement the FPGA version.

Planned, architected and managed and delivered full ASIC emulation and bring up projects for NXP, Netlogic, etc.

Experienced High Density and high-speed FPGA Architecture and Verilog & Board Design including ASIC Verification using Altera and Xilinx with high speed Serdes.

Created initial product requirements & specs of the iCompression MPEG2 codec chip. The world's first single chip Audio/Video Data Encoder and TS Mux chip. Located engineers to be the founders and seeded iCompression through NUKO Information Systems. ***iCompression sold for $500M to Globespan.***

Went from white board drawings to functioning Apollo 8000 nit Dolby Vision® proof of concept monitor including PCB Design, layout fab and assembly and debug in 8 weeks. Project was demonstrated to movie labs and cable labs to show the future of TV's. It was the basis for multimillion-dollar annual licensing to companies like Panasonic, Sony and Canon

Joined Dolby at their request to deliver fully functional HDR monitor demo to CES in 10 weeks. Internal group wanted 7 months to architect, design and have a PCB ready for CES with their team of 8. Single handedly delivered working system from scratch 2 weeks ahead of CES.

Created and designed all the hardware for the Liquid Cooled Pulsar, 6000 nit Dolby Vision monitor. Still considered the only Hollywood approved grading monitor 9 years running.

Co-designed, Product Planned and Specified the **world's first** ever MP2 player chip.

Led Samsung and Panasonic design teams to implement **the world's first MPEG players**, leading to their early dominance in the DVD market.

Designed the first few MPEG 1 & 2 Set Top Boxes in the Industry.

Called in for Emergency Consulting. Took over design from a team of 6. Single handedly re-architected, re-designed, implemented and debugged and reliability tested in **6 weeks**, a complete Backplane Proprietary IP Packet MAC in a space & speed limited FPGA for Metro Area Network (MAN) and Resilient Packet Ring (RPR) implementation. Allowed company to demo on schedule and ship MAN products ahead of any other company.

Within 2 weeks of joining C-Cube, found cause & designed a work around for an interface flaw in the, (at the time) sole income providing, chip that design engineers had spent 4 months trying to find. *Fixing this problem saved project with* ***Philips*** *and restored* ***a multimillion-dollar chip contract.***

In 4 months started up and established a fully functional applications group to support new SPARC RISC chipset, (SparKIT). As Applications Manager, recruited and trained 9 engineers. Developed evaluation boards for customer training and chip debug, installed Customer Hotline, databases, started FAE magazine named FAEdback, to train over 100 LSI Logic international applications engineers. Did shows, developed and produced customer training seminars around the world. Brought the world's first 21 Customer SPARCstation Clones to market and seeded the SPARCstation clone market (till SUN killed it).

Designed the world's first digitized Video Transmission over Fiber

Designed the world's first MPEG over DS2/D23/SONET transmission

Designed the world's first MPEG over ATM over ADSL transmission

Through persuasive and innovative action gained company approximately $150,000 by making available rare but necessary machinery for sorting wafers so sales could be achieved.

Successfully cut through bureaucracy to resolve the problem of transferring mask plates between wafer fabrication areas. Saved company over $500,000 in mask costs.

Pinpointed procedural error in fabrication process which eliminated repeat occurrence of the problem; saving company up to $250,000.

PROFESSIONAL EXPERIENCE

Tentmaker Systems Consulting Group, San Jose, CA **2018-**
Chief Technology Officer

- Customers like T3, Dolby Labs, Light Field Labs, Ventex etc.

Dolby Labs, Sunnyvale, CA **2008-2018**
Senior Staff Engineer

- HW architect and designer for every Dolby Vision HDR monitor and AR/VR design made by Dolby which allowed us to make HDR and Dolby Vision the major accepted Technology world over and launched a steady multimillion annual stream of Licensing income.
- Went on to design the very first Quantum Dot Display monitor for Dolby. This allowed QD Monitors to become standardized bringing additional licensing revenue in excess of $50M.
- Author and co-author of 5 Dolby Patents. Helped Ensure Dolby's continued technology leadership and licensing portfolio

Tentmaker Systems, San Jose, CA **2002-2008**
Chief Technologist

Responsible for Sales, International coordination, Architecture, Project management and Customer Satisfaction

- Developed sales to $1.6M in consulting revenues per year
- Local team of 4, India team of 6-8. RTL, Board Design, Firmware & Software.
- Customers included Xilinx, JDSU, Brilliant, Netlogic Microsystems, Mentor Graphics, Reliancy, BBNC, Stream Processors, Philips Semiconductor (various groups within Philips)/NXP, WIS Technologies (various fill in roles within WIS), DataRobotics, Audience, Varian Medical Systems.

Propulsion Networks, Campbell, CA **2001-2002**
Co-Founder, Chief Architect and VP of Technology

- Raised $15M in VC Funding
- Recruited 18 engineers, ASIC Designers, Verification, PCB design, Software, Firmware, Standards.
- Conceived, worked with potential customers to Define, Propose, Architect a Metro/Core Router 40G/10G Network Processor ASIC.
- All schedules met. Fully functional gate level C-Model demonstrated. Received lots of customer enthusiasm and validation. Applied for 16 patents (currently owned by Intel). The VC's opted to close down the company & sell off the IP when they realized our product was 10 years ahead of its time.

Luminous Networks, Cupertino, CA **1999-2001**
Director, ASIC Design

Requested by the CEO to take over the ASIC group responsible for the ASIC version of the LMAC. Managed 8 RTL & Verification Engineers. Took the design to a fully functional Simulation.

- Left to start Propulsion Networks per prior agreement with CTO & CEO.

Principal Architect, Office of the CTO

- Responsible for re-architecture and re-design (Verilog) of the LMAC. Core MAC unit for the RPR Resilient Packet Ring.
- Co-author of 3 Luminous patents

Bay Micro Systems, San Jose, CA **1998-1999**
Co-founder with Rick Blezynski

- Raised first round $3M in Venture Funding through my personal VC contacts. BMI is still in operation today. Engineered the Bay architecture and used that to raise funding.

NUKO Information Systems, San Jose, CA **1994-1998**
Chief Technology Officer & VP of Engineering
Chief Technology Officer
Chief Technologist

Director of Engineering

- Raised $70M in funding based on my architecture
- Hired over 40 Engineers and 60 employees, Engineering included 2 Directors, 5 managers, RTL, Board Design, Layout and Library Engineering, Mechanical, Documentation, Technicians, Support Engineers. Setup an entire documentation system from scratch for our products with ECNs (change order notification) and AVLs etc to manage the engineering part of the production flow.
- Wrote and managed the documentation and operation manuals for our systems
- Developed training for our Sales Staff and Support Engineers (after doing Customer Support myself)
- Interfaced with major Contract Manufacturing houses to set up and stage production.
- Pioneered the first MPEG Video Transmission over Phone Lines using PacBell's DS2/DS3 networks.
- Architected the first MPEG over ATM over DSL transmission systems.

ADDITIONAL PROFESSIONAL EXPERIENCE

C-Cube Microsystems, Milpitas, CA
Manager, System Design and Applications

LSI Logic, Milpitas, CA
Manager, SPARC Applications Engineering, SPARC Division
Senior Staff Member, Applications, DSP Division.

Advanced Micro Devices, Sunnyvale, CA
Sr. Product Planning & Applications Strategic Development Engr, High Speed Serial & Optical Networking Development Group.
Product Engineer, Microprocessors Division.

UC Berkeley Extension
Instructor

EDUCATION

Master of Science Electrical Engineering (**MSEE)**, Computer Engineering and Solid-State Physics, Oregon State University
Bachelor of Science Electrical Engineering (BSEE), Electrical Engineering and Computer Engineering, Oregon State University

SOCIETIES AND AWARDS

- 6-time winner of Dolby Idea Quest Awards (for Innovation) in 9 years, a number went on to become products.
- Wyle / EE Times American By Design Contest, 1st Place Design Winner for Digital Devices.
- Wyle / EE Times Idea Quest Grand Prize Winner. Winner of Saturn EV1 Electric Vehicle.
- NUKO Employee elected Summit Award Winner (2 time)
- President, Tau Beta Pi OR Alpha Chapter, Engineering Honor Society
- Eta Kappa Nu, Electrical Engineering Honor Society
- Chairman, IEEE Student Organization, OSU
- 2x Teaching Assistant of the Year Award, Engineering Dept, OSU (by Student Vote)

SERVICE ACTIVITIES

- MOD Night - Coordinate and manage an extracurricular activity involving over 120 volunteers and over 480 Junior High students in one / two night "Outward Bound" style Night Game Ministry activity spread out around the Santa Cruz, CA and Portland, OR mountains. (Prior to 2001).
- Counselor/Mentor for High School and Junior High Youth (since 1985).

Partial list of Patents (applied, pending or granted)

Click to follow links

Systems and Methods for Display Systems Having Improved Power Profiles

Variable flower display backlight system

Method and apparatus for using multiple network processors to achieve higher performance networking applications

Method of policing network traffic

Apparatus and method for queuing flow management between input, intermediate and output queues

Mechanism for distributing statistics across multiple elements

Adapting video images for wearable devices

Passive Multi-Wearable-Devices Tracking

Augmented 3d entertainment systems

Method and apparatus for packet segmentation, enqueuing and queue servicing for multiple network processor architecture

Packet classification method

Method and apparatus for a network processor having an architecture that supports burst writes and/or reads

Detecting bit errors in a communications system

Business method for selling advertisements and traffic related services on electronic billboards

Method and apparatus for managing multiple data flows in a content search system

Partial list of Architecture and Designs

Boards, Systems and FPGAs. Unless indicated, includes End to end, Conception, Systems Architecture, Board and FPGA Architecture, Design, FW, and support. Covers some of the items mentioned above as well:

Dolby HDR and Dolby Vision Boards (partial list): Contrast, Phoenix, Lanai, Pulsar, Pulsar II, Maui, Apollo (numerous other projects in the AR/VR field still confidential).
TAXIcab : TAXIchip Circuit Application Board: First high speed Serdes
TAXIvideo : TAXIchip Video Transmission Board: First Ever Demo of Digitized Video over Optical Fiber
Saavik 1 & 2: LSI Logic MPEG 2 over DS2 ISA Decoder board.
Spock I : 9U VME Audio/Video Multiplexing board
Spock III : 8 input Transport Stream Multiplexing board designed using FPGAs.
Sarek III : 9U VME C-Cube MPEG 2 Encoder board. Multiple FPGAs.
DV-MPEG : Hot-swappable NORTEL Chassis Codec System (6U) consisting of the 4 boards below.
Riker : IBM MPEG 2 Encoder board
William : Hot-swap NORTEL Motherboard for above Encoder.
Troi : C-Cube Decoder Board
Deanna : Hot-swap NORTEL Motherboard for above Decoder.
Atlas : 9U VME Fully Redundant mother board for a full featured Codec
Sammy : 9U VME Video Input, Audio Encoder, MPEG TS muxer board
Uhura : 9U VME 9 channel ATM TS multiplexer over OC3c or DS3
Aruhu : 9U VME 9/36 channel ATM TS demultiplexer over OC3c or DS3
Highlander : Multi-Redundant 44/40 U chassis 9 channel 9U Codec system
iCompression Single Chip Encoder
: Primary Systems level definition for the iCompression Single Chip MPEG 2 Encoder, also initiated the founding of iCompression and gave them $2M startup to provide me with a substitute for the C-Cube encoder. iCompression sold for $500M
Picard : iCompression Encoder PCI board.
ReMuxer : Architect of the MPEG2/ATM Multi-Re-multiplexer System and Chassis
TPM1 FPGA: DIVA Systems Transport Processor Module,
Completely re-architected and redesigned their Transport Processor FPGA.
TPMII : DIVA Systems Transport Processor Board II.
Architected the second generation of the DIVA board for Video on Demand. Architected and designed the core FPGA, the M4SPROC, a 4 stream MPEG TS processor.
TPMtester : DIVA Systems Tester board.
Architected, designed, debugged this large test board with multiple connectors and connections to allow a fast test and bring-up environment for the DIVA TPMII boards.
DVB2MII : Luminous Video TS DVB to Ethernet Board including all FPGAs. Implemented a module to convert and reconvert Video TS to IP over Ethernet to allow it to be transmitted over any 100baseT network. Board and FPGA was used for demo systems at shows and was used to capture a critical investment.
LMAC 1G :Luminous Backplane MAC FPGA. Multiple flavors of this FGPA were shipped in all Luminous Products, with multiple per card and upto 6 on the Switch Card.
LMAC 2.5G: Luminous Backplane MAC FPGA. This FPGA was shipped in all 2.5G Luminous products.
VIP Interface: FPGA that interfaces MPEG TS and I2S and SPDIF to a VESAVIP bus.
PCI to HPI bus interface: FPGA that interfaces PCI to local bus. Includes CCIR656 Interface to PCI, interface ensures ability to preview with VCR FF and REW inputs.
PCIexpress Northstar III: Implementation of Xilinx core for proof of concept. Done in 12 weeks to demo with working video.
PCIexpress FPGA/ASIC Verification suite of boards: Validation of PCIe and Video ASIC RTL in FPGA
PCIexpress ASIC board: Validation board for PCIe ASIC chip with video.
Multiple other PCIe designs.
(Multiple other Consulting designs not listed as all recent designs are confidential).